REMARKS/ARGUMENTS

The previously pending claims have been canceled and have been replaced with the current new set of claims comprising claims 65-74. No new matter has been added. Further examination and reconsideration of the application, as amended, are requested. Applicants are also submitting the accompanying Information Disclosure Statement with a citation to U.S. Patent No. 6,757,201 to Matsuda et al.

Amendments to the Specification

With regard to the specification, the Examiner requested update of the Summary of the Invention to reflect the current claims. Therefore, Paragraph 16 of the application as filed has been deleted and replaced with the text in this document, based on the newly submitted claim 65. The Examiner also requested correction of Paragraph 19, Brief Description of the Drawings, to reflect the drawing figures of the application. Such corrective amendments are presented with this document.

The Invention and New Claims

The invention is directed to controlling memory access by providing a first memory write operation and a second memory write operation, wherein the write speed of the first write operation is different from the speed of the second write operation. For example, the specification describes performing a first write operation as a fast write and performing a second write operation as a slow write (see Paragraphs 75-77 of the specification). Various write modes of operation can be provided, including fast and slow writes, cache writes, and address-based writes with address specified in registers (see Paragraphs 73-81). Determining when to perform a fast write and when to perform a slow write can be based on the address space to which a write operation is directed. See, for example, Fig. 14-16 and accompanying specification.

In other aspects of the invention, the write operations can include first, second, third, and fourth modes in which the write operation to non-volatile memory (e.g. EEPROM) is a fast write operation (first mode), or is a slow write operation (second mode), or is fast or slow depending on the write address area (third mode), or is a cache write to RAM (fourth mode).

Thus, a system constructed in accordance with the invention can access an EEPROM in multiple write modes of operation and the write access time can be changed in accordance with the write mode.

It is submitted that the newly presented claims are not anticipated nor rendered obvious by any of the references of record. For example, the newly cited publication to Tobita (US2002/0051394) describes a controller in Fig. 48 that connects three flash modules in which two modules are slow-access flash memory 1239 and one module is fast-access flash memory 1014. The writing speed, however, is fixed according to the flash memory module and therefore Tobita does not teach changing the access speed based on an operation mode (including fast access mode and slow access mode). In addition, Tobita does not teach a change in write access operation from accessing the non-volatile (EEPROM) memory to accessing the cache memory based on the operation mode.

It is submitted that none of the references, taken alone or in combination, teaches or suggests the novel feature of the invention relating to changing the access speed of a write operation to non-volatile memory in accordance with operation mode.

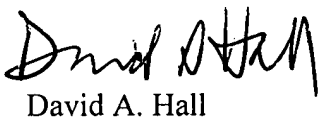
Information Disclosure Statement (IDS)

The Examiner objected to the IDS filed October 28, 2003 because the IDS does not include the number of the application for which the IDS is being submitted (Page 2 of the Office Action). The pending application was filed on October 28, 2003. It is noted that the IDS in question was filed on that date, concurrently with the application papers. Hence, no application number was assigned at the time and therefore it was impossible for applicants to include the application number on the IDS document. It is submitted that the IDS filed October 28, 2003 was in compliance, to the extent possible, with all pertinent requirements at the time of filing the IDS. Withdrawal of the objection to the IDS and acceptance on the merits of the October 28, 2003 IDS filed with the application papers is respectfully requested.

CONCLUSION

In view of the foregoing, Applicants believe all claims 65-74 now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

Respectfully submitted,



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